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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
MYERS, PAUL R

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 02/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.		Applicant(s)
Office Action Summary	09/964,805		BARMORE, BRAD A.
	Examiner		**Art Unit**
	Paul R. Myers		2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>29 November 2004</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All   b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
     Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments with respect to claims 1-22 have been considered but are moot in

view of the new ground(s) of rejection.

Applicants argument that Lehwalder teaches configuring codecs based on which codec is

enabled/disabled and not based upon which the codec support capability of the codec controller

is persuasive. The newly added reference to Caugherty teaches selecting codecs based on the

codecs supported by digital signal processing software (Column 3 lines 5-16).

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lehwalder et

al PN 6,609,170 in view of Caugherty PN 6,597,702.

As per claim 1, Lehwalder discloses a riser comprising: a plurality of riser codecs (21a-

c); and an adaptive initialization module (signal control circuit) coupled to the riser codecs, the

initialization module to configure (col. 4, lines 47-67) the riser codecs when the riser is

connected to a motherboard having a codec controller (4) and a primary codec (20); said

initialization module to automatically select between a first multi-codec configuration and a

second multi-codec configuration based on a codec support capability of the codec controller

(col. 4, lines 62-67). Lehwalder selects codecs to configure based upon which codecs are

enabled/disabled. Lehwalder does not does not teach selecting codecs to configure based upon

the support capability of the codec controller. Caugherty teaches selecting codecs based upon

the support capability of the codec controller (the DSP Column 3 lines 5-16). It would have been

obvious to a person of ordinary skill in the art at the time of the invention to select the codec

based upon the support capability of the codec controller because this would have prevented

selecting a unsupported codec.

As per claim 2, Lehwalder discloses the riser of claim 1 wherein the first multi-codec

configuration is a two-codec configuration (2 secondary codecs) and the second multi-codec

configuration is a three-codec configuration (3 secondary codecs).

As per claim 3, Lehwalder discloses the riser of claim 2 wherein the initialization module

includes: a detection module (e.g. routing module) to monitor a status of a signal (e.g. reset

signal; or Presence indicator); and an address controller (ID Decoder module) coupled to the

detection module and the riser codecs; said address controller to select a two-codec address

structure when the signal status indicates that the codec controller supports up to two codecs and

a three-codec address structure when the signal status indicates that the codec controller supports

up to three codecs (col. 9, lines 10-45).

As per claim 4, Lehwalder discloses the riser of claim 3 wherein the signal status

indicates whether data is to be delivered from the primary codec to the codec controller in a two-

codec configuration (col. 9, lines 47-65).

As per claim 5, Lehwalder discloses the riser of claim 3 wherein the three-codec address

structure includes: a first address corresponding to the primary codec; a second address

corresponding to a first riser codec; and a third address corresponding to a second riser codec (e.g. col. 9, lines 10-65).

As per claim 6, Lehwalder discloses the riser of claim 3 wherein the initialization module further includes an enabling mechanism (Reset signal) coupled to the primary codec, the enabling mechanism to disable the primary codec when the codec controller supports up to two codecs.

As per claim 7, Lehwalder discloses the riser of claim 6 wherein the two-codec address structure includes: a first address corresponding to a first riser codec; and a second address corresponding to a second riser codec (e.g. col. 9, lines 10-65).

As per claim 8, Lehwalder discloses the riser of claim 2 further including: a printed wiring board (e.g. motherboard) electrically connecting the riser codecs to the initialization module; and a connector (connector 5) coupled to the printed wiring board, the connector enabling electrical communication between the riser and the motherboard (figs. 1-2).

As per claim 9, Lehwalder discloses the riser of claim 8 wherein the connector has a data delivery pin, the data delivery pin enabling the initialization module to determine the codec support capability of the codec controller (presence indicator; fig. 2).

As per claim 10, Lehwalder discloses an adaptive initialization module, the initialization module comprising: a detection module (routing module; col. 8, lines 47-67) to monitor a status of a signal; and an address controller (ID decoder module) coupled to the detection module; said address controller to select a two-codec address structure when the signal status indicates that the codec controller supports up to two codecs and a three-codec address structure when the signal status indicates that the codec controller supports up to three codecs (col. 4, lines 60-67).

As per claim 11, Lehwalder discloses the initialization module of claim 10 wherein the signal status indicates whether data is to be delivered from a primary codec to the codec controller (presence indicator; signals whether the primary codec is enabled or not so as to send signals to the controller; fig. 2).

As per claim 12, Lehwalder discloses the initialization module of claim 10 wherein the three-codec address structure includes: a first address corresponding to the primary codec (col. 7, lines 38-39); a second address corresponding to a first riser codec (e.g. col. 7, lines 39-45); and a third address corresponding to a second riser codec (e.g. col. 7, lines 39-45).

As per claim 13, Lehwalder discloses the initialization module of claim 10 further including an enabling mechanism (Reset signal) coupled to the primary codec, the enabling mechanism to disable the primary codec when the codec controller supports up to two codecs (e.g. col. 9, lines 10-45).

As per claim 14, Lehwalder discloses the initialization module of claim 13 wherein the two-codec address structure includes: a first address corresponding to a first riser codec (first secondary codec); and a second address corresponding to a second riser codec (second secondary codec).

As per claim 15, Lehwalder discloses a riser (2) comprising: a plurality of riser codecs (fig. 2); a detection module (routing module) to monitor a status of a signal where the signal status indicates whether data is to be delivered from a primary codec to a codec controller (presence indicator; signals whether the primary codec is enabled or not so as to send signals to the controller; fig. 2); an address controller (ID decode module) coupled to the detection module and the riser codecs, said address controller to select a two-codec address structure (2 secondary

codecs) when the control signal indicates that the codec controller supports up to two codecs

(primary on the motherboard is disabled) and a three-codec address structure (3 secondary

codecs; when the primary on the motherboard is enabled) the control signal indicates that the

codec controller supports up to three codecs; a printed wiring board (motherboard) electrically

connecting the riser codecs to the detection module and address controller (figs. 1 and 2); and a

connector (connector 5) coupled to the printed wiring board, the connector enabling electrical

communication between the riser and a motherboard (col. 9, lines 10-65).

As per claim 16, Lehwalder discloses the riser of claim 15 wherein the connector has a

data delivery pin (presence indicator), the data delivery pin enabling the riser to determine a

codec support capability of the codec controller (presence indicator; signals whether the primary

codec is enabled or not so as to send signals to the controller; fig. 2).

As per claim 17, Lehwalder discloses a method of configuring a plurality of riser codecs,

the method comprising: monitoring a status of a signal where the signal status indicates whether

data is to be delivered from a primary codec to a codec controller ; (presence indicator; signals

whether the primary codec is enabled or not so as to send signals to the controller; fig. 2);

selecting a two-codec address structure (2 secondary codecs) when the signal status indicates that

the codec controller supports up to two codecs; and selecting a three-codec address structure (3

secondary codecs) when the signal status indicates that the codec controller supports up to three

codecs (e.g. col. 10-65).

As per claim 18, Lehwalder discloses the method of claim 17 further including

determining whether a data delivery pin of a connector (5) is terminated (presence indicator;

disabled), the connector coupling a riser containing the riser codecs to a motherboard containing

the primary codec and the codec controller (fig. 2).

As per claim 19, Lehwalder discloses the method of claim 17 further including: placing

the primary codec at a first address (e.g. 00); placing a first riser codec at a second address (e.g.

01); and placing a second riser codec at a third address (e.g. 10).

As per claim 20, Lehwalder discloses the method of claim 17 further including: disabling

the primary codec (hold in reset; fig. 2); placing a first riser codec at a first address (primary;

00); and placing a second riser at a second address (secondary 01; col. 9, lines 10-45).

As per claim 21, Lehwalder discloses a computer-readable storage medium storing a set

of instructions (BIOS), the set of instructions capable of being executed by a processor to

configure a plurality of riser codecs, the method comprising: monitoring a status of a signal

where the signal status indicates whether data is to be delivered from a primary codec to a codec

controller (presence indicator signal); selecting a two-codec address structure (2 secondary

codecs) when the signal status indicates that the codec controller supports up to two codecs; and

selecting a three-codec address structure (3 secondary codecs) when the signal status indicates

that the codec controller supports up to three codecs (e.g. col. 9, lines 10-67).

As per claim 22, Lehwalder discloses the computer-readable storage medium of claim 21

wherein the method further includes determining whether a data delivery pin of a connector (5)

is terminated (disabled), the connector coupling a riser (2) containing the riser codecs (21a-c) to

a motherboard (1) containing the primary codec (20) and the codec controller (4; fig. 2).

Conclusion

4.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The

examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

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system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRM
February 10, 2005

PAUL R. MYERS
PRIMARY EXAMINER